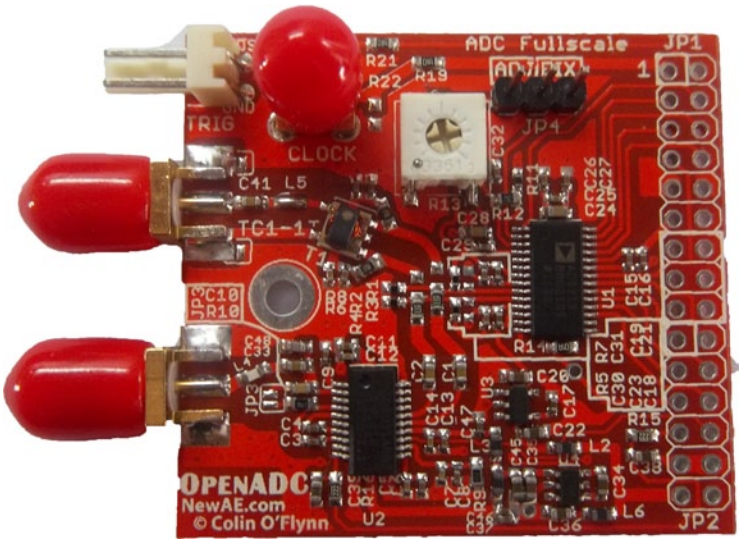
OPENADC

Product Datasheet

The OpenADC is a simple Analog to Digital Converter (ADC) add-on suitable for most FPGA development kits. The OpenADC features a flexible input architecture which makes it suitable for a variety of tasks. The entire design is available for reference, including several FPGA reference projects and computer-based capture software.

Features

- **105 MSPS ADC**
- **Two input options: Low Noise Amplifier or Transformer**
- **400 MHz analog bandwidth (transformer)**
- **40 MHz analog bandwidth (amplifier)**
- **Software adjustable gain on Low Noise Amplifier (-5 to 55 dB)**
- **Adjustable ADC reference voltage**
- **SMA Connector for external clock input**
- **Separate voltage regulators for ADC & LNA**
- **Digilent Pmod™ Compatible Headers, and also fits many other popular FPGA boards**
- **Extensive factory test procedure**
- **2.25 - 3.6V Digital I/O Compatible**



The OpenADC when combined with a FPGA provides a complete capture architecture. The following figure shows what such a capture architecture would include. Note the OpenADC board alone does not provide all these functions, the user is responsible for providing them through a FPGA board. A sample design is available which shows how these could be provided.

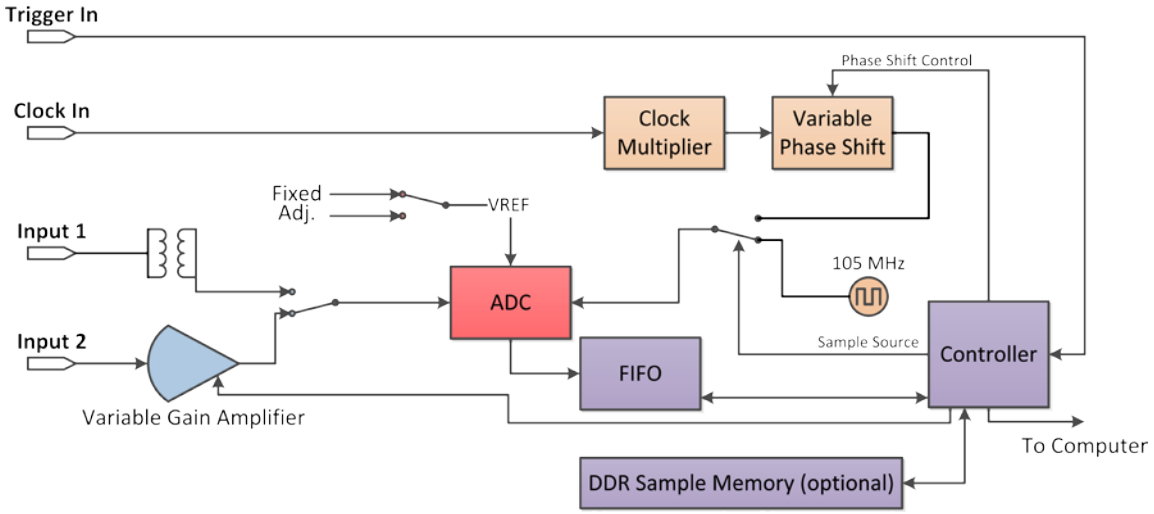


Fig 1. Complete capture application the OpenADC makes possible.

Typical Specifications

Frequency Response

The following two figures show the attenuation over frequency for the two input options. The source signal was a -1.0 dBm signal, and the sampling rate of the OpenADC was 40.000 MHz. This 40.000 MHz sample clock was provided by the signal generator.

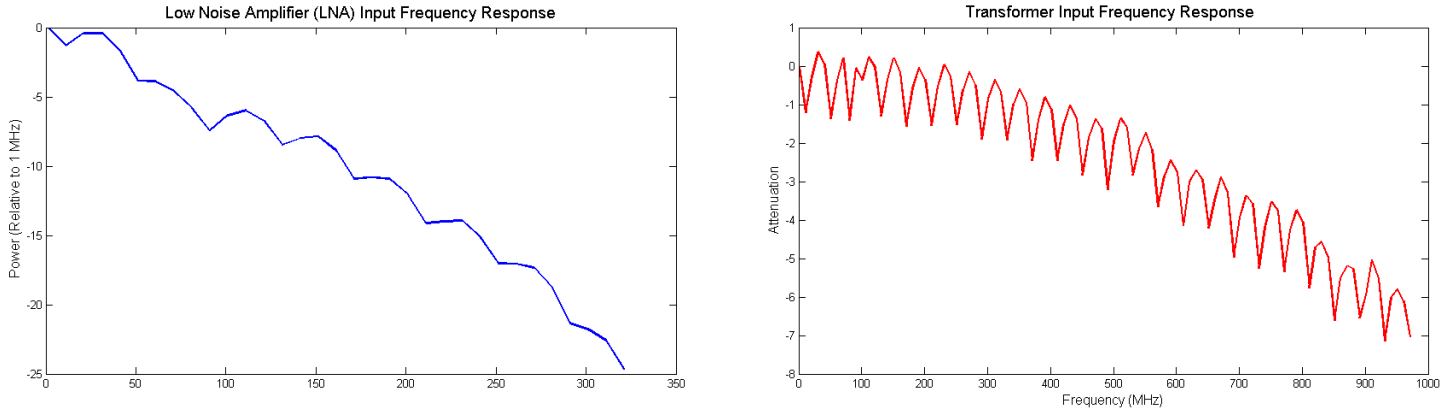


Fig 2. Examples of high-frequency roll-off. The LNA bandwidth an be increased by removing C49, at the expense of worse input matching characteristics. The 40.000 MHz sample rate is responsible for the 'bumps' in this graph.

Input Matching (S11 Parameter)

The following two figures show the S11 parameter measured at both the LNA input connector and the transformer input connector. These can be adjusted by the user to target a better match over a specific frequency range.

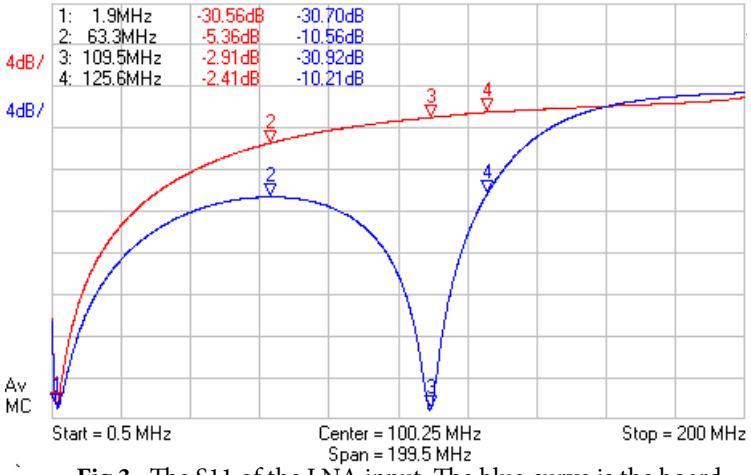


Fig 3. The S11 of the LNA input. The blue curve is the board as delivered. The red curve is with C49 removed to show the effect of this capacitor value.

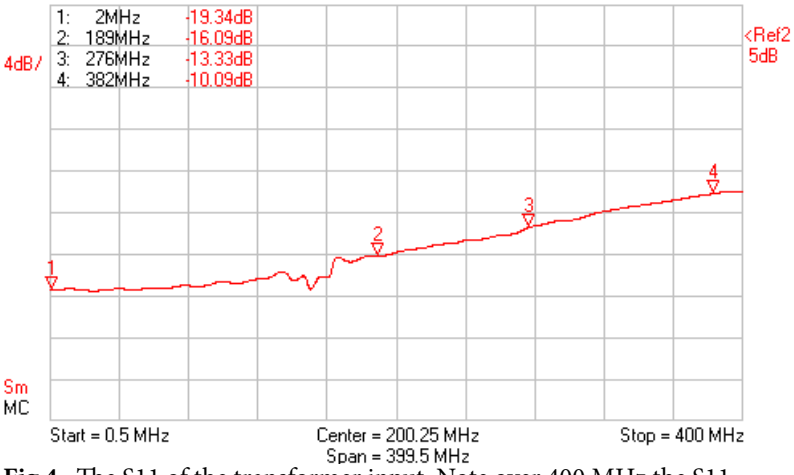
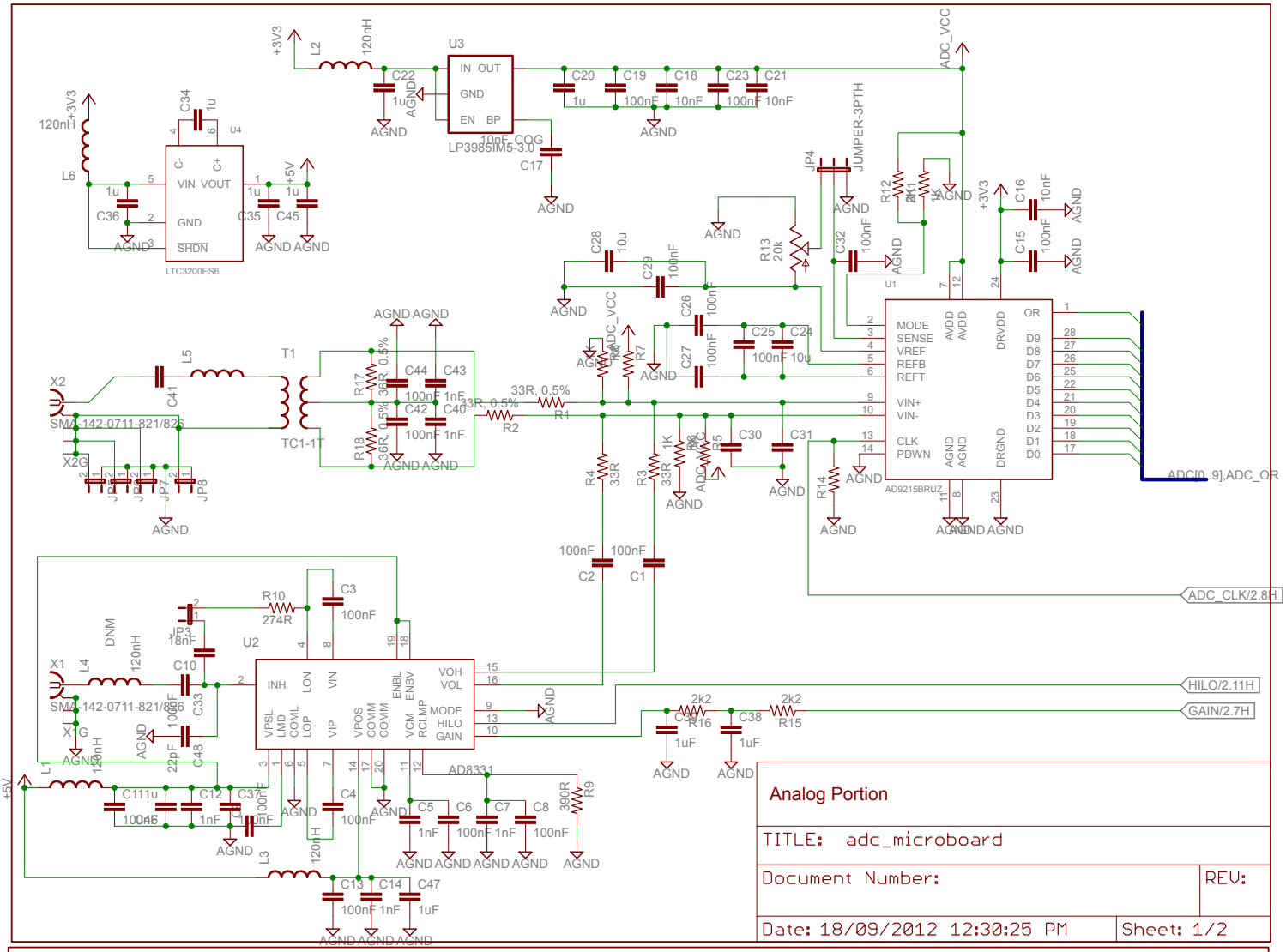
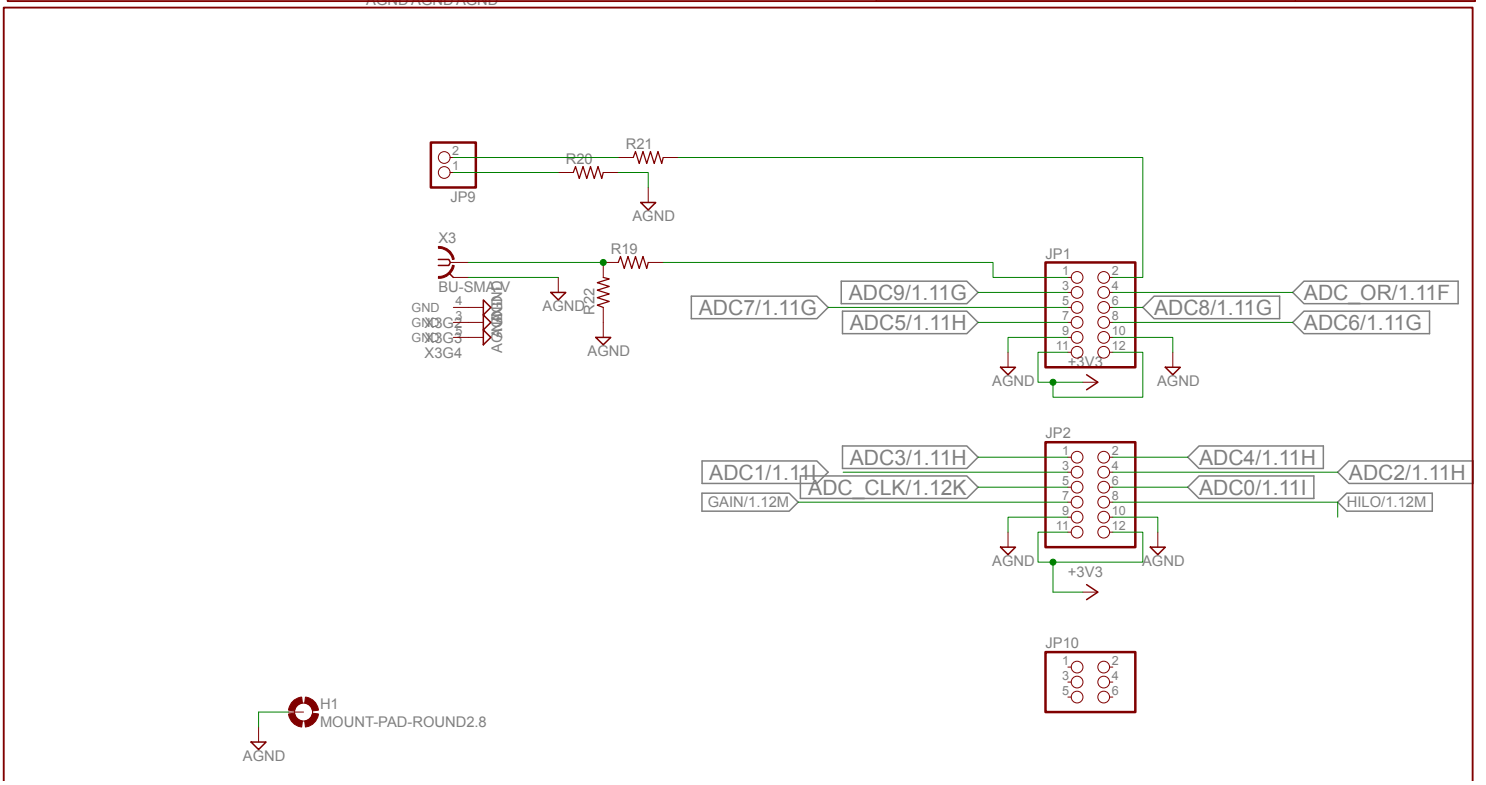


Fig 4. The S11 of the transformer input. Note over 400 MHz the S11 is better than -10 dB.

Schematic

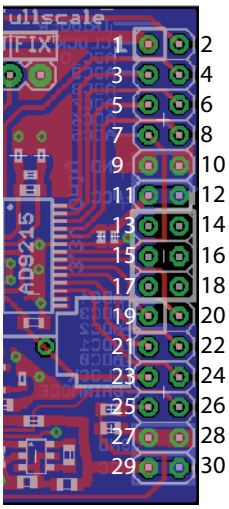

Analog Portion
TITLE: adc_microboard
Document Number:
REV:
Date: 18/09/2012 12:30:25 PM
Sheet: 1/2
ADC_CLK/2.8H
HILO/2.11H
GAIN/2.7H
ADC[0..9],ADC_OR
LP3985IM5-3.0
LTC3200ES6
AD9215BRUZ
AD8331


JP9
X3
BU-SMA-V
JP1
JP2
JP10
ADC7/1.11G
ADC9/1.11G
ADC5/1.11H
ADC8/1.11G
ADC_OR/1.11F
ADC6/1.11G
ADC1/1.11I
ADC3/1.11H
ADC_CLK/1.12K
ADC4/1.11H
ADC2/1.11H
ADC0/1.11I
GAIN/1.12M
HILO/1.12M
H1
MOUNT-PAD-ROUND2.8

FPGA Interface & Usage Notes

Pinout

The pinout & associated pin function is shown below. This is viewed from the top of the board:



Pin Number	Pin Function		Pin Function	Pin Number
1	SMA to FPGA (Clock In)		Trigger Input to FPGA	2
3	ADC9		ADC_OR	4
5	ADC7		ADC8	6
7	ADC5		ADC6	8
9	GND		GND	10
11	DVCC (+2.25V to +3.6V)		DVCC(+2.25V to +3.3V)	12
13	No Connection		No Connection	14
15	No Connection		No Connection	16
17	No Connection		No Connection	18
19	ADC3		ADC4	20
21	ADC1		ADC2	22
23	ADC Clock		ADC0	24
25	LNA Gain Voltage (PWM)		LNA Gain Mode (Hi/Low)	26
27	GND		GND	29
29	AVCC (+3.1V* to 4.5V)		AVCC (+3.1V* to 4.5V)	30

The 'No Connection' pins have no internal connection. When connecting to FPGA boards they may be used as 'spares' to route signals onto other pins.

Clock Input

The 'Clock In' can be used to feed an external clock into the FPGA. This pin may alternatively be used for any other purpose - for example feeding a signal out on the SMA connector. Two resistor pads are provided in series & parallel with this SMA connector, which may be used for termination purposes.

This signal may not route to a dedicated FPGA clocking resource. In many applications this will be acceptable, since the clock may only be used to generate the sample clock for the ADC. There will be many additional delays which will need to be compensated for in the ADC sample chain, thus the delay added by the non-dedicated clock resource is irrelevant. **Note there is no ESD or over-voltage clamping provided, carefully check your host board to see if this should be added**.

Trigger Input

The trigger input can be used as a trigger input for the system. **Note there is no ESD or over-voltage clamping provided, carefully check your host board to see if this should be added**.

ADC Data, Overrange, and Clock

The ADC is configured to output data in 'offset binary' mode. See the AD9215 datasheet for more detailed information about possible ADC output configurations. The ADC has a 'duty cycle stabilizer' enabled by default - certain applications which require a changing sample rate may need to disable this feature. See the AD9215 datasheet for more details.

The clock must range from 5 to 105 MHz. Parallel termination of the clock line at the ADC is done with a 100-ohm resistor. Note there will be some delay between the FPGA setting the clock high and data being present at the FPGA inputs. The FPGA designer must account for this delay - for example if attempting to clock the external data inputs on the rising edge of the internal FPGA clock, this may fail due to the delay in FPGA output buffers, and the delay in FPGA input buffers. A pad is provided in the ADC clock path which can be connected to a FPGA pin. This would provide a feedback path for the clock - this path will have the same delay as the ADC data signals (output buf + input buf), so data could be clocked on the rising edge of this 'feedback' clock.

* The AVCC pin range can be adjusted to 2.5V-4.5V with a solder jumper change. See 'Summary of PCB Options'.

FPGA Interface & Usage Notes

LNA Gain Mode & Gain Voltage

The AD8331 Low Noise Amplifier is controlled by two pins. One selects the gain mode, either 'high' or 'low'. The other selects the exact gain amount. The gain voltage pin is designed to be driven by a PWM signal, and will be filtered on the OpenADC to apply a voltage varying from 0.0 to 1.0V. When driving this pin with normal 3.3V logic, the maximum duty cycle of the PWM pin will thus be 30.3%. **Do not exceed 2.5V at the AD8331 device or it will be damaged.**

Transformer Input

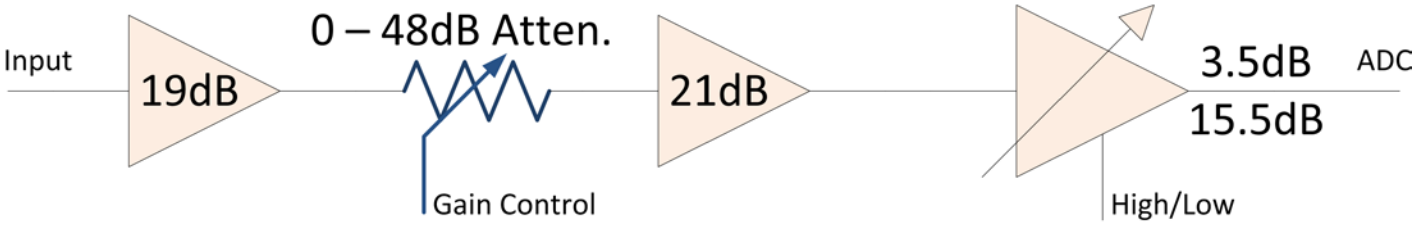
The transformer input is designed to present a 50-ohm impedance. The optional inductor L5 can be used to improve the matching over a specific frequency range. The typical S11 response is shown in figure 4.

The transformer input by default does not connect the SMA shield to system ground. This can be used to break ground loops between different pieces of equipment. If desired, four solder jumpers are provided which can be used to connect the SMA shield to the system ground.

Low Noise Amplifier Input

The LNA input is designed to present either a 50-ohm or 6K-ohm impedance. With a few component changes can provide other impedances, see the AD8331 datasheet. If jumper JP3 is bridged (factory default), the input impedance is 50-ohm. If JP3 is open, the input impedance is 6K-ohm.

Care must be taken to avoid clipping internally in the AD8331 (LNA) device. The equivalent circuit of the LNA is shown below. Note that the adjustable gain is provided with an attenuator, the result of this is the maximum input power is limited to avoid clipping in the intermediate stages. The suggested maximum input signal for the LNA input is -1.8 dBm or 0.635 Vp-p. See AD8331 datasheet for more information.



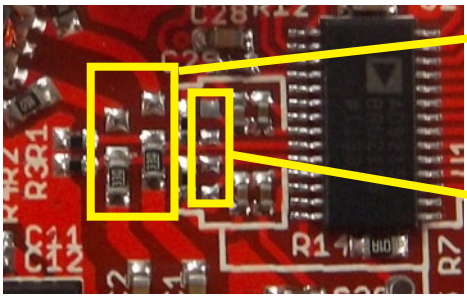
ADC Filtering Setup

Capacitors C30 and C31 can be used to provide low-pass filtering on the ADC input. They are not mounted by default as they would hamper undersampling applications.

ADC Voltage Reference

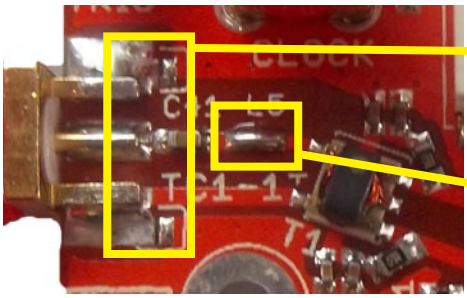
The ADC (AD9215) can be configured for a full-scale reading of anywhere from 2V p-p to 1V p-p. If jumper JP4 is in the 'fix' location the ADC is configured for 2V p-p full-scale using an internal precision reference. If jumper JP4 is set to the 'adj' position, and R13 is rotated fully clockwise, the ADC is configured for a 1V p-p full scale using an internal precision reference. If jumper JP4 is set to the 'adj' position, and R13 is not rotated fully clockwise, the ADC will be configured for a full-scale varying from 1V p-p to 2V p-p depending on the position of resistor R13.

Summary of PCB Solder Jumpers & Options



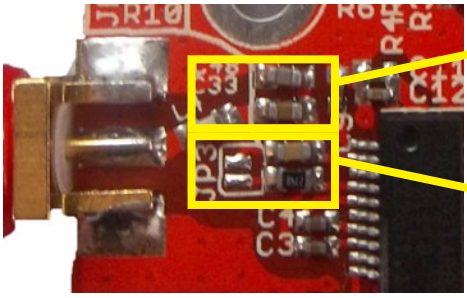
These pads select if the input to the ADC comes from the transformer or the LNA. Using solder jumpers instead of a switch allows good high-frequency response for low cost. As shown the LNA is enabled, to enable the transformer carefully move the resistors to the upper pad.

Capacitors can be mounted here to filter out high-frequency signals before reaching the ADC. If using the ADC in Nyquist-limited applications these should be mounted.



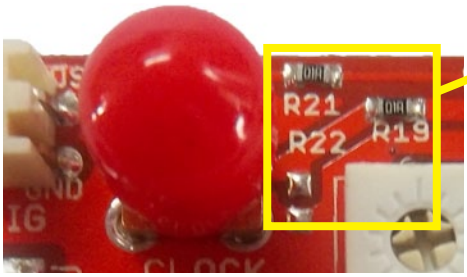
Four solder jumpers (2 top side, 2 bottom side) connect the SMA shield to the system ground. Leave these open to eliminate ground loops.

L5 can be adjusted to create better matching at specific frequencies. For best wideband performance this is shorted.



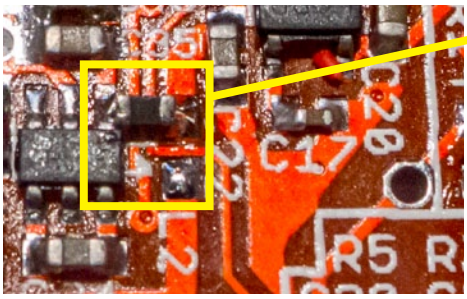
C49 and L4 can be adjusted to provide better matching and to adjust the high-frequency roll-off.

If JP3 is open the input is high-impedance (6K-ohm). If JP3 is shorted the input impedance is set with C10 & R10. The default value of C10 & R10 results in a 50-ohm input impedance, which will be less sensitive to noise than a high-impedance input.



R22 provides parallel termination for the SMA Clock connector.

R21, R19, and R20 (backside) provide resistive isolation of the trigger & clock signals. They can be combined with a diode clamp on the FPGA board to provide ESD protection.



By default the 3.0V rail for the ADC is regulated from the AVCC pin, requiring at minimum 3.1V on the AVCC pin.

L2 can be moved as here to take power from the output of the 5V boost converter. This allows you to power the AVCC pin from as low as 2.5V. The entire OpenADC can be run from a 2.5V system with this change.

Example Applications

Verilog FPGA Code

Verilog HDL code is provided for the FPGA target. The example code targets a Spartan 6 device, although the code can easily be ported to any Xilinx target. It can easily fit in a small device such as a Spartan 3A-200, the size of the device primarily defines how large the sample buffer is. Further examples show how to use DDR memory and also how to download data over Ethernet.

Compiled bitstreams for the Avnet LX9 Microboard are provided for users that only wish to use the board for capture purposes.

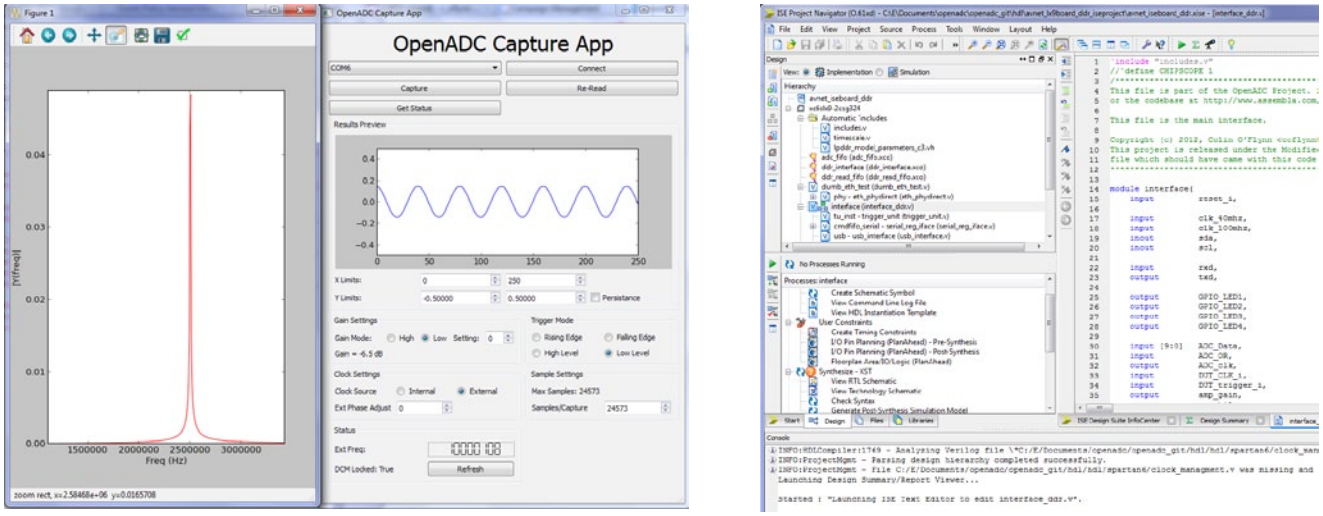


Fig 5. Example FPGA code in Verilog is provided to show how a capture application can work. In addition a Python based interface is provided which demonstrates downloading the data, along with a simple frequency analysis window. This can be extended for a variety of applications.

Python Interface

A python interface shows how to connect to the board, change settings, and get data. A PySide based GUI is also available which can be extended for a variety of applications.

Supported Hardware

The only officially supported FPGA board is the Avnet LX9 Microboard. Any FPGA board that can interface to 2.25 - 3.6V logic can be used. Xilinx-based boards will simplify porting the example code over, but any vendor FPGA should be interoperable with the OpenADC board. Note the ADC digital I/O voltage must be at least 2.25V. If interfacing to a 1.8V part, check if it will accept higher input levels. If so the OpenADC may interface directly.

Fig 6. The Avnet LX9 Microboard

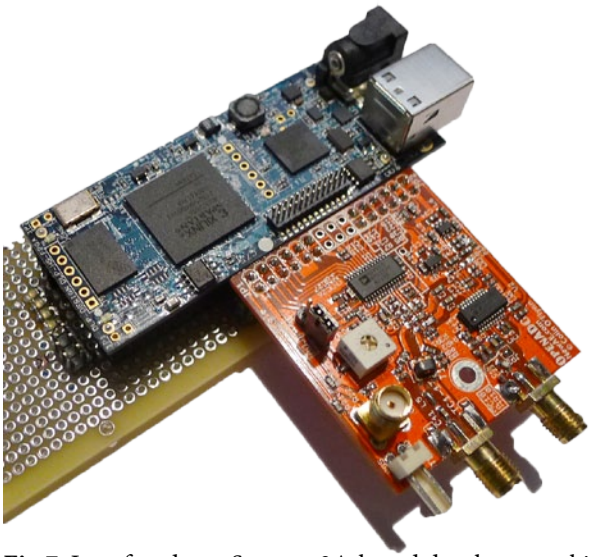


Fig 7. Interfaced to a Spartan 3A-based development kit.

Downconversion & Undersampling Applications

What are Undersampling Applications?

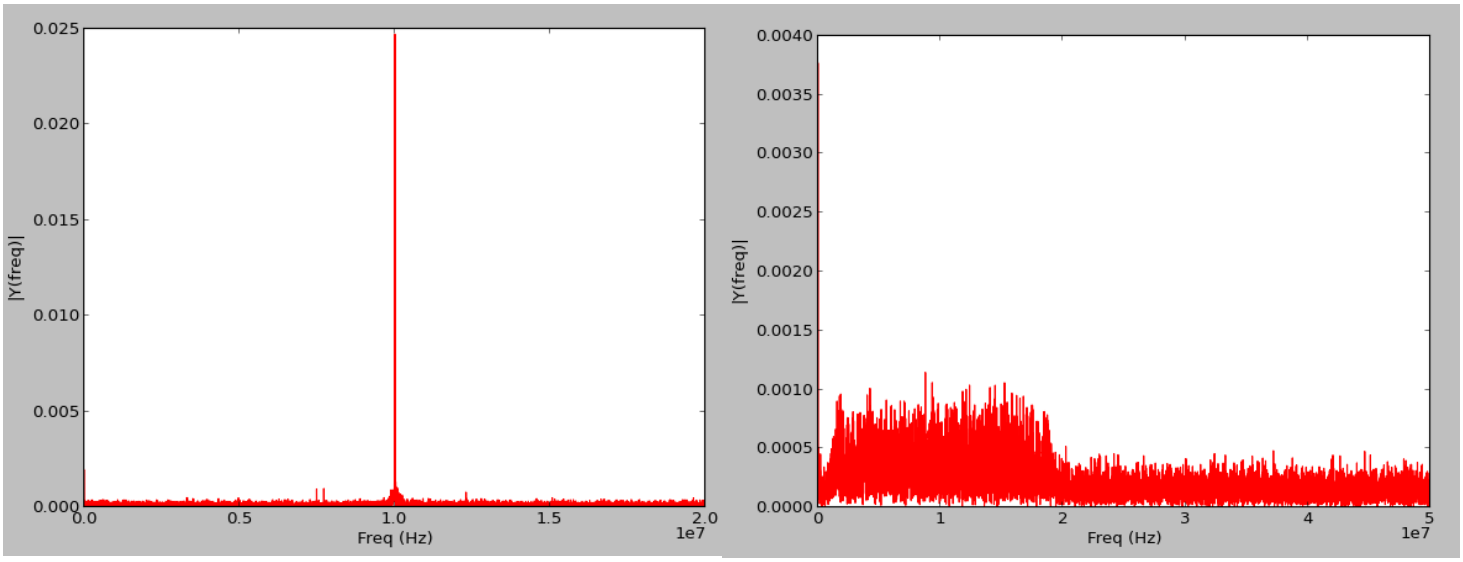
Typical ADC or acquisition boards contain a Nyquist filter. This filter is designed to remove frequency components higher than half the sample frequency. Any frequency above this point will be aliased back into the measurement in a typically undesirable way.

The OpenADC does not have a Nyquist filter mounted. This allows you to sample slower than the frequency components of interest! If you measure a 110 MHz signal at 100 MHz, the result will look like a 10 MHz signal. Taking advantage of this requires you to be knowledgeable about the input spectrum, since both a 210 MHz and a 110 MHz signal would look the same when sampled at 100 MHz. Typically filters will ensure you don't have unexpected signals mixing together, such as only passing signals around 210 MHz.

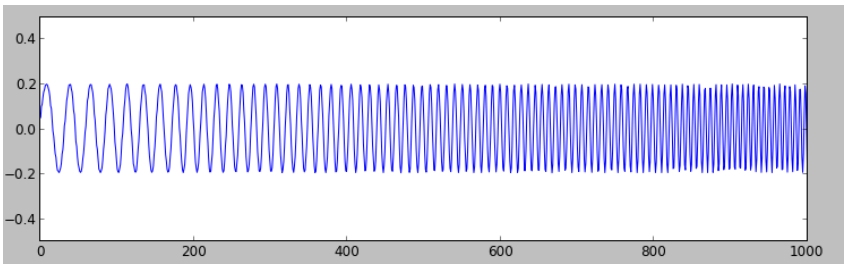
Inputs and Clocks

The transformer input provides the best wide-band performance. You can use the LNA input at high frequencies - you just may need to add additional gain to compensate for roll-off. The following figure measures a 410 MHz signal using the LNA - notice we need to add 43.7 dB of gain. This will of course amplify low-frequency signals considerably more, so the input spectrum must be very pure (nothing at low frequencies).

When using undersampling applications, you also must ensure clocks are synchronized. For both the two figures below we have generated a 410 MHz signal from a signal generator. The spectrum on the left is sampled at 40.000 MHz, where that 40.000 MHz clock is derived from the 10.000 MHz reference of the signal generator. The signal on the right is sampled at 100.00 MHz generated from an internal crystal oscillator.



The following figure shows a time-domain representation of the signal measured in the above case when sampling with the 100.00 MHz oscillator. In the time domain it can easily be seen that a beat frequency exists between the two oscillators - when using the ADC in downconverting (undersampling) applications, careful consideration of the clock source must be given. Generally you will require a sample clock phase-locked to the signal being measured.



Revision History

Oct 20, 2012
Initial Release

Nov 6, 2012
Update to include ability to power from 2.7V, update digital IO voltage range

Sept 7, 2014
Gain Mode / Gain Voltage pins were swapped in table.